410 Rec'd PCT/PTO 12 SEP 2001

°FORM PTO-1390 (REV 11-2000) OFFICE — U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. § 371

ATTORNEY'S DOCKET NUMBER: 44912-20097.00

U.S. APPLICATION NO. (If known, see 37 CFR 1.5): 09/936290 NOT YET ASSIGNED

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE00/00614	March 1, 2000	March 12, 1999

TITLE OF INVENTION

TRANSCEIVER HAVING DIGITAL SIGNAL SIGNAL PROCESSING

APPLICANT(S) FOR DO/EO/US

Thomas MOLIERE

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☒ The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☒ is attached hereto (required only if not communicated by the International Bureau).
   b. ☐ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application under PCT Article 19 (35 U.S.C. 371(c)(2)).
   a. ☒ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☒ Other items or information: 1. International Search Report 2. IPER 3. Return receipt postcard.

CERTIFICATE OF HAND DELIVERY

I hereby certify that this correspondence is being hand filed with the United States Patent and Trademark Office in Washington, D.C. on May 25, 2001.

Melissa Garton

Melissa Garton

U.S. APPLICATION NO (if known, see 37 CFR 1.5) NOT YET ASSIGNED 09/936290	INTERNATIONAL APPLICATION NO. PCT/DE00/00614	ATTORNEY'S DOCKET NUMBER: 44912-20097.00

21. ☒ The following fees are submitted:

BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5)):

Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO $1,000.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO $860.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO $710.00

International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provision of PCT Article 33(1)-(4) $690.00

International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00

	CALCULATIONS PTO USE ONLY	
ENTER APPROPRIATE BASIC FEE AMOUNT =	$860.00	
☐ Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$0	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	10 - 20 =	0	x $18.00	$0	
Independent claims	1 - 3 =	0	x $80.00	$0	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $270.00	$0	
TOTAL OF ABOVE CALCULATIONS =				$860.00	

☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by ½.	$0	
SUBTOTAL =	$0	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +	$0	
TOTAL NATIONAL FEE =	$0	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00 per property** +	$0	
TOTAL FEES ENCLOSED =	$860.00	
	Amount to be refunded:	**$**
	charged:	**$860.00**

a. ☒ The Commissioner is hereby authorized to charge $860.00 and any additional fees that may be required, or credit any overpayment to **Deposit Account No. 03-1952**. Reference Docket Number 44912-20097.00

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Kevin R. Spivak
Morrison & Foerster LLP
2000 Pennsylvania Avenue, N.W.
Washington, D.C. 20006-1888

SIGNATURE

Kevin R. Spivak
Registration No. 43,148

PATENT
Docket No. 44912-20097.00

CERTIFICATE OF HAND DELIVERY

I hereby certify that this correspondence is being hand filed with the United States Patent and Trademark Office in Washington, D.C. on September 12, 2001.

Melissa Garton

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Thomas MOLIERE

Serial No.: Not yet assigned

Filing Date: September 12, 2001

For: TRANSCEIVER HAVING DIGITAL SIGNAL PROCESSING

Examiner: Not yet assigned

Group Art Unit: Not yet assigned

PRELIMINARY AMENDMENT

BOX PCT
Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination on the merits, please amend this application as follows:

In the Specification:

Page 1 before the first paragraph, please delete the following:

~~Description~~

Page 1 before the first paragraph, please insert the following:

TRANSCEIVER HAVING DIGITAL SIGNAL PROCESSING

Page 1, before the first paragraph, please insert the following heading and insert:

Claim for Priority

This application claims priority to International Application No. PCT/DE00/00614 which was published in the German language on September 21, 2000.

Page 1, between lines 1 and 2 please insert the following heading:

TECHNICAL FIELD OF THE INVENTION

Please replace the paragraph beginning on line 2 of page 1 with the following rewritten paragraph:

The invention relates to a transceiver having an RF receiver, and in particular, to a transceiver having a UHF receiver.

Page 1, between lines 11 and 12 please insert the following heading:

BACKGROUND OF THE INVENTION

Please replace the paragraph beginning on line 17 of page 1 with the following rewritten paragraph:

GSM devices operate, for example, in the 900 MHz band. In conventional embodiments, the receiver has an intermediate frequency of 45 - 400 MHz and the transmitter operates with direct modulation of a carrier which is generated on the transmission frequency. A channel oscillator and a fixed frequency oscillator both use a 13 MHz crystal oscillator as a reference. The frequency of 13 MHz is used because the clock frequency which is required centrally by the GSM digital part relates to 13 MHz with 13/6 = 2.1666 MHz, and the channel raster frequency of 200 kHz, which is equal to the comparison frequency of the channel synthesizer, is also derived from it by simple frequency division. 13 MHz is thus the lowest possible reference oscillator frequency of each conventional GSM telephone.

Please replace the paragraph beginning on line 33 of page 1 with the following rewritten paragraph:

The seventy-second harmonic of the 13 MHz oscillator occurs in the 936 MHz reception channel, and the seventy-third harmonic occurs in the 949 MHz reception channel. In mobile phones which are highly miniaturized, the spatial proximity of the radio modules to the receiver input and to the antenna results in a particular problem. Current specifications prescribe that interference frequencies at the 50 ohm receiver input must be less than 0.7 micro volts, for example. A customary 13 MHz crystal oscillator oscillates at an amplitude of approximately 1 volt, which means that harmonics of this oscillator may appear damped by more than 120 dB in the 900 MHz region at the receiver input. However, the high-speed silicon transistors which are customary today give rise to upper harmonic intervals of only approximately 60 dB in relation to the useful carrier in the 900 MHz region. Additional damping between the crystal oscillator and the receiver input of approximately 60 dB is thus necessary. Given the small spatial distances between these regions of at most 40 mm, this gives rise to an extreme level of expenditure on shielding in customary GSM mobile phones, i.e. to the use of sheet metal parts, metal housing etc. Attempts at solving this harmonic problem by means of switching measures alone, for example by means of harmonic filters, have only been partially successful because the harmonics are generally reflected by them and not destroyed, which in an extreme case can even lead to a situation in which critical harmonics are irradiated in an amplified form.

On page 1, between lines 25 and 26 please insert the following heading and paragraphs:

SUMMARY OF THE INVENTION

In one embodiment of the invention, there is a transceiver. The transceiver includes, for example, an RF receiver with digital signal processing in a digital part with an input part, at least one mixer, and an intermediate frequency/baseband processing device having a local channel oscillator to which a first phase locked loop with a phase discriminator and an adjustable first frequency converter are assigned, and having a reference oscillator for the phase locked loop and the control clock of the digital signal processing device, wherein in order to acquire the control clock, a digital clock synthesizer is provided to which an upward signal of the reference oscillator is supplied, and a control signal is supplied by the digital part in the form of a digital tuning word, the frequency of the reference oscillator being selected such that its order of magnitude is at least equal to the bandwidth of one or more of the reception bands used and harmonics do not occur in a reception channel.

In another aspect of the invention, the clock synthesizer is a synthesizer with direct digital synthesis.

In another aspect of the invention, the first frequency converter is a DDS synthesizer or a fractional N divider with a sigma-delta modulator.

In yet another aspect of the invention, a fine-tuning signal is supplied to the first frequency converter by the digital part.

In another aspect of the invention, there is an IF oscillator to which a second phase locked loop with a phase discriminator and a second frequency converter is assigned, an output signal of the reference oscillator being supplied to the phase discriminator, and a modulation signal and a fine-tuning signal being supplied to the frequency converter by the digital part.

In yet another aspect of the invention, the frequency converter assigned to the IF oscillator is a DDS synthesizer or a fractional N divider with sigma-delta modulator.

In still another aspect of the invention, the modulation signal is supplied to the IF oscillator frequency converter from the digital part.

In yet another aspect of the invention, the modulated IF signal is generated using frequency conversion, frequency division or DDS.

In another aspect of the invention, the transceiver is a homodyne receiver in which the modulated RF carrier, and a direct or rearranged output signal of the local channel oscillator are supplied to a reception mixer so that the intermediate frequency corresponds to the baseband.

In still another aspect of the invention, the modulated output signal of the IF oscillator and the output signal of a transmission mixer are fed to a phase discriminator, to which a signal of a controlled transmission oscillator and an output signal of the local channel oscillator are supplied.

Brief Description of the Drawings

The invention, together with further advantages, is explained in more detail below with reference to an exemplary embodiment which is illustrated in the drawing.

Figure 1 shows a basic, simplified block diagram of a transceiver according to the invention.

Detailed Description of the Preferred Embodiments

The invention discloses a transceiver having an RF receiver, and in particular, to a transciever having a UHF receiver, with a digital signal processing device in a digital part, with an input part, at least one mixer and an intermediate frequency/baseband processing means, and having a local channel oscillator to which a first phase locked loop with a phase discriminator

and an adjustable first frequency converter are assigned, and having a reference oscillator for the phase locked loop and the control clock of the digital signal processing device.

Please replace the paragraph beginning on line 26 of page 2 with the following rewritten paragraph:

The invention provides a transceiver in which the aforesaid problem with harmonics of the reference oscillator is solved to the effect that costs, volume and weight of the device are reduced by eliminating or decreasing the expenditure on shielding.

Please replace the paragraph beginning on line 32 of page 2 with the following rewritten paragraph:

This is achieved with a transceiver according to the invention. In order to acquire the control clock, a digital clock synthesizer is provided to which an output signal of the reference oscillator and a control signal are fed from the digital part in the form of a digital tuning word, the frequency of the reference oscillator being selected such that its order of magnitude is at least equal to the bandwidth of one or more of the reception bands used, and harmonics do not occur in a reception channel.

Please replace the paragraph beginning on line 3 of page 3 with the following rewritten paragraph:

The invention prevents harmonics occurring in a reception channel, with the result that the shielding between the transmitter part and receiver part can be significantly reduced.

Please replace the paragraph beginning on line 8 of page 3 with the following rewritten paragraph:

In one embodiment, the clock synthesizer is embodied as a synthesizer with direct digital synthesis because as a result any frequency can be generated from any other frequency, and the frequency can also be finely adjusted.

Please replace the paragraph beginning on line 13 of page 3 with the following rewritten paragraph:

A further embodiment has a first frequency converter which is a fractional N divider with a sigma-delta modulator. This embodiment provides the advantage that it permits high-speed channel changes, fine-tuning and good phase changing values with high comparison frequencies even with a conventional structure.

Please replace the paragraph beginning on line 26 of page 3 with the following rewritten paragraph:

Another embodiment of the invention is defined in that an IF oscillator is provided to which a second phase locked loop with a phase discriminator and a second frequency converter is assigned, an output signal of the reference oscillator being supplied to the frequency discriminator, and a modulation signal and a fine-tuning signal being supplied to the frequency converter. As a result, a modulated signal can be advantageously conditioned. It may be advantageous here if a GMSK modulation signal of a finely adjustable sigma-delta synthesizer is supplied to the IF oscillator.

Please replace the paragraph beginning on line 1 of page 4 with the following rewritten paragraph:

The invention permits the use of both the conventional heterodyne receiver and of a homodyne receiver in which the modulated RF reception signal and an output signal, in each case with the latter's frequency, of the channel synthesizer are fed to a reception mixer so that the intermediate frequency corresponds to the baseband.

Please delete the paragraph beginning on line 15 of page 4.

Please replace the paragraph beginning on line 21 of page 4 with the following rewritten paragraph:

According to Figure 1, a transceiver according to the invention includes a controller MPR and a baseband processing device BBV, which are illustrated in a single block designated as digital part DIT. A reference oscillator REO, which supplies an output signal S_{REF} is provided in a known fashion, and the signal is then used in the way described below to acquire a control clock and to derive the channel frequencies necessary for the transceiver and transmitter. The output signal S_{REF} is then supplied to a digital synthesizer DDS, which expediently operates in accordance with digital direct synthesis. Such synthesizers are known, and a modern exemplary embodiment is described in the company literature CMOS, 125 MHz Complete DDS Synthesizer, AD 9850, Analog Devices, Inc. 1998, together with circuitry examples and functional explanations. In such a DDS synthesizer, any frequency can generate any desired other frequency, and fine adjustment is also possible using an AFC signal so that cheaper oscillators of any desired frequency, even ceramic oscillators or freewheeling oscillators,

can be used as the reference oscillator. Reference oscillators have until now been one of the most expensive modules in radio telephones owing to the necessary precision and stability.

Please replace the paragraph beginning on line 9 of page 5 with the following rewritten paragraph:

The synthesizer DDS supplies a control clock f_{STE} to a micro controller of the digital part DIT, and receives from said block a control signal S_{AFC}, namely in the form of a digital tuning word, which both brings about the frequency conversion and the fine tuning to the precise clock frequency, which is carried out using a precise clock received from the base station, namely in the form of a digital tuning word. The output signal S_{REF} of the reference oscillator REO is also fed to a phase lock loop which includes a first frequency converter FU1, a phase discriminator PD1, a low-pass filter, TP1 and a local channel oscillator EVO. The frequency converter FU1 is expediently embodied as a fractional N divider with sigma-delta modulator, and it receives a fine-tuning signal h_{AFC} and a channel signal S_{KAN} from the microprocessor block MPR, BBV. The output signal of the channel oscillator EVO is fed at the receiver end to a receiver mixer EMI. The radio-frequency signal S_{HAM} is supplied to this receiver mixer, the radio-frequency signal S_{HAM} passing via an antenna ANT with a controllable change-over switch AUS, a bandpass filter BP2 and a low-noise amplifier LNA. Mixing is expediently carried out directly into the baseband, in accordance with modern concepts, i.e. the frequency of the mixing oscillator signal corresponds precisely to the frequency of the radio-frequency signal S_{HAM}. The oscillator frequency at the mixer input can be the same as the direct frequency of the oscillator EVO, or equal to a frequency of the oscillator EVO which is converted, for example by means of a frequency converter. Receivers operating according to this

principle are known as homodyn receivers. A detailed description of a signal-delta fractional N synthesizer can be found in "Delta-Sigma Modulation in Fractional-N Frequency Synthesis", EEE Journal of Solid-State Circuits, Vol. 28, No. 5, May 1993, pp 553-559.

Please replace the paragraph beginning on line 5 of page 6 with the following rewritten paragraph:

At the transmitter end, the output signal S_{EVO} of the channel oscillator EVO is fed to a transmitter mixer SME. The transmitter mixer is included in a phase locked loop which includes a controlled transmission oscillator SVO, a phase discriminator PD3 and a low-pass filter TP3, and a signal h_{MOD} is also supplied to the (third) phase discriminator PD3, in addition to the output signal S_{SMI}.

Please replace the paragraph beginning on line 13 of page 6 with the following rewritten paragraph:

The signal h_{MOD} constitutes the modulated output signal of an IF oscillator ZFO, which is likewise included in a (second) phase locked loop which also includes a second frequency converter FU2, a second phase discriminator PD2 and a second low-pass filter TP2. A modulation signal S_{MOD} and a fine-tuning signal g_{afc} are fed to the frequency converter FU2 by the microprocessor and baseband blocks MPR, BBV, and the output signal of the frequency converter FU2 passes to an input of the phase discriminator PD2 whose other input is supplied with the output signal S_{REF} of the reference oscillator REO.

In the Claims:

What is claimed is:

1. (Amended) A transceiver, comprising:

an RF receiver with a digital signal processing device in a digital part with an input part;

at least one mixer; and

an intermediate frequency/baseband processing device having a local channel oscillator to which a first phase locked loop with a phase discriminator and an adjustable first frequency converter are assigned, and having a reference oscillator for the first phase locked loop and a control clock of the digital signal processing device,

wherein in order to acquire the control clock (f_{STE}), a digital clock synthesizer is provided to which an upward signal of the reference oscillator is supplied, and a control signal is supplied by the digital part in the form of a digital tuning word, the frequency of the reference oscillator being selected such that its order of magnitude is at least equal to the bandwidth of one or more of the reception bands used and harmonics do not occur in a reception channel.

2. (Amended) The transceiver as claimed in claim 1, wherein the clock synthesizer is a synthesizer with direct digital synthesis.

3. (Amended) The transceiver as claimed in claim 1 wherein the first frequency converter is a DDS synthesizer or a fractional N divider with a sigma-delta modulator.

4. (Amended) The transceiver as claimed in claim 1, wherein a fine-tuning signal is supplied to the first frequency converter by the digital part.

5. (Amended) The transceiver as claimed in claim 1, further comprising an IF oscillator to which a second phase locked loop with a phase discriminator and a second frequency converter is assigned, an output signal of the reference oscillator being supplied to the phase discriminator, and a modulation signal and a fine-tuning signal being supplied to the frequency converter by the digital part.

6. (Amended) The transceiver as claimed in claim 1, wherein the frequency converter assigned to the IF oscillator is a DDS synthesizer or a fractional N divider with sigma-delta modulator.

7. (Amended) The transceiver as claimed in one claim 1, wherein the modulation signal is supplied to the IF oscillator frequency converter from the digital part.

8. (Amended) The transceiver as claimed in claim 1, wherein the modulated IF signal is generated using frequency conversion, frequency division or DDS.

9. (Amended) The transceiver as claimed claim 1, wherein the transciever is a homodyne receiver in which the modulated RF carrier, and a direct or rearranged output signal of the local channel oscillator are supplied to a reception mixer so that the intermediate frequency corresponds to the baseband.

10. (Amended) The transceiver as claimed in claim 5, wherein the modulated output signal of the IF oscillator and the output signal of a transmission mixer are fed to a phase discriminator, to which a signal of a controlled transmission oscillator and an output signal of the local channel oscillator are supplied.

In the Abstract:

Please replace the original Abstract with the substitute Abstract attached herewith.

REMARKS

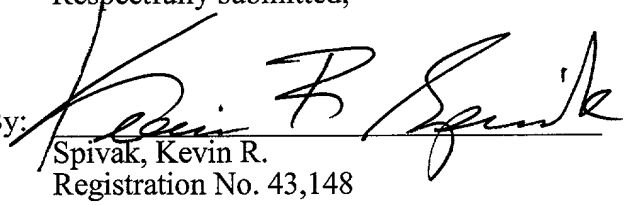
The above amendments to the specification, claims and abstract have been made to place the application in proper U.S. format and to conform with proper grammatical and idiomatic English. None of the amendments herein are made for reasons related to patentability. No new matter has been added.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**".

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 44912-20097.00. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Respectfully submitted,

Dated: September 12, 2001

By: 

Spivak, Kevin R.
Registration No. 43,148

Morrison & Foerster LLP
2000 Pennsylvania Avenue, N.W.
Washington, D.C. 20006-1888
Telephone: 202-887-6924
Facsimile: (202) 263-8396

VERSION WITH MARKINGS TO SHOW CHANGES MADE

For the convenience of the Examiner, the changes made are shown below with deleted text in strikethrough and added text in underline.

In the Specification:

Page 1 before the first paragraph, has been amended to delete the following:

~~Description~~

Page 1 before the first paragraph, has been amended to include the following Title:

TRANSCEIVER HAVING DIGITAL SIGNAL PROCESSING

Page 1, before the first paragraph, has been amended to include the following heading and insert:

Claim for Priority

This application claims priority to International Application No. PCT/DE00/00614 which was published in the German language on September 21, 2000.

Page 1, between lines 1 and 2, has been amended to include the following heading:

TECHNICAL FIELD OF THE INVENTION

Paragraph beginning on line 2 of page 1 has been amended as follows:

The invention relates to a transceiver having an RF receiver, and in particular, to a transceiver having a UHF receiver~~, with digital signal processing means in a digital part, with an input part, at least one mixer and an intermediate frequency/baseband processing means, and having a local channel oscillator to which a first phase locked loop with a phase discriminator~~

~~and an adjustable first frequency converter are assigned, and having a reference oscillator for the phase locked loop and the control clock of the digital signal processing means.~~

Page 1, between lines 11 and 12, has been amended to include the following heading:

BACKGROUND OF THE INVENTION

Paragraph beginning on line 17 of page 1 has been amended as follows:

GSM devices operate, for example, in the 900 MHz band~~., and in~~ In conventional embodiments, the receiver has an intermediate frequency of 45 - 400 MHz and the transmitter operates with direct modulation of a carrier which is generated on the transmission frequency. A channel oscillator and a fixed frequency oscillator both use a 13 MHz crystal oscillator as a reference~~., the~~ The frequency of 13 MHz ~~being~~ is used because the clock frequency which is required centrally by the GSM digital part relates to 13 MHz with 13/6 = 2.1666 MHz, and the channel raster frequency of 200 kHz, which is equal to the comparison frequency of the channel synthesizer, is also derived from it by simple frequency division. 13 MHz is thus the lowest possible reference oscillator frequency of each conventional GSM telephone.

Paragraph beginning on line 33 of page 1 has been amended as follows:

The seventy-second harmonic of the 13 MHz oscillator occurs in the 936 MHz reception channel, and the seventy-third harmonic occurs in the 949 MHz reception channel. In ~~particular in~~ mobile phones which are highly miniaturized, the spatial proximity of the radio modules to the receiver input and to the antenna results in a particular problem. Current specifications prescribe that interference frequencies at the 50 ohm receiver input must be less

than 0.7 micro volts, for example. A customary 13 MHz crystal oscillator oscillates at an amplitude of approximately 1 volt, which means that harmonics of this oscillator may appear damped by more than 120 dB in the 900 MHz region at the receiver input. However, the high-speed silicon transistors which are customary today give rise to upper harmonic intervals of only approximately 60 dB in relation to the useful carrier in the 900 MHz region. Additional damping between the crystal oscillator and the receiver input of approximately 60 dB is thus necessary. Given the small spatial distances between these regions of at most 40 mm, this gives rise to an extreme level of expenditure on shielding in customary GSM mobile phones, i.e. to the use of sheet metal parts, metal housing etc. Attempts at solving this harmonic problem by means of switching measures alone, for example by means of harmonic filters, have only been partially successful because the harmonics are generally reflected by them and not destroyed, which in an extreme case can even lead to a situation in which critical harmonics are irradiated in an amplified form.

Page 1, between lines 25 and 26, has been amended to include the following heading and paragraphs:

SUMMARY OF THE INVENTION

In one embodiment of the invention, there is a transceiver. The transceiver includes, for example, an RF receiver with digital signal processing in a digital part with an input part, at least one mixer, and an intermediate frequency/baseband processing device having a local channel oscillator to which a first phase locked loop with a phase discriminator and an adjustable first frequency converter are assigned, and having a reference oscillator for the phase locked loop and the control clock of the digital signal processing device, wherein in order to acquire the control

clock, a digital clock synthesizer is provided to which an upward signal of the reference oscillator is supplied, and a control signal is supplied by the digital part in the form of a digital tuning word, the frequency of the reference oscillator being selected such that its order of magnitude is at least equal to the bandwidth of one or more of the reception bands used and harmonics do not occur in a reception channel.

In one aspect of the invention, the clock synthesizer is a synthesizer with direct digital synthesis.

In another aspect embodiment of the invention, the first frequency converter is a DDS synthesizer or a fractional N divider with a sigma-delta modulator.

In yet another aspect of the invention, a fine-tuning signal is supplied to the first frequency converter by the digital part.

In another aspect of the invention, there is an IF oscillator to which a second phase locked loop with a phase discriminator and a second frequency converter is assigned, an output signal of the reference oscillator being supplied to the phase discriminator, and a modulation signal and a fine-tuning signal being supplied to the frequency converter by the digital part.

In yet another aspect of the invention, the frequency converter assigned to the IF oscillator is a DDS synthesizer or a fractional N divider with sigma-delta modulator.

In still another aspect of the invention, the modulation signal is supplied to the IF oscillator frequency converter from the digital part.

In yet another aspect of the invention, the modulated IF signal is generated using frequency conversion, frequency division or DDS.

In another aspect of the invention, the transciever is a homodyne receiver in which the modulated RF carrier, and a direct or rearranged output signal of the local channel oscillator are supplied to a reception mixer so that the intermediate frequency corresponds to the baseband.

In still another aspect of the invention, the modulated output signal of the IF oscillator and the output signal of a transmission mixer are fed to a phase discriminator, to which a signal of a controlled transmission oscillator and an output signal of the local channel oscillator are supplied.

Brief Description of the Drawings

The invention, together with further advantages, is explained in more detail below with reference to an exemplary embodiment which is illustrated in the drawing.

Figure 1 shows a basic, simplified block diagram of a transceiver according to the invention.

Detailed Description of the Preferred Embodiments

The invention discloses a transceiver having an RF receiver, and in particular, to a transciever having a UHF receiver, with a digital signal processing device in a digital part, with an input part, at least one mixer and an intermediate frequency/baseband processing means, and having a local channel oscillator to which a first phase locked loop with a phase discriminator and an adjustable first frequency converter are assigned, and having a reference oscillator for the phase locked loop and the control clock of the digital signal processing device.

Paragraph beginning on line 26 of page 2 has been amended as follows:

~~An object of the~~ The invention ~~is therefore to~~ provides a transceiver in which the aforesaid problem with harmonics of the reference oscillator is solved to the effect that costs, volume and weight of the device are reduced by eliminating or decreasing the expenditure on shielding.

Paragraph beginning on line 32 of page 2 has been amended as follows:

This ~~object~~ is achieved with a transceiver ~~of the type mentioned at the beginning in which,~~ according to the invention, ~~in~~ In order to acquire the control clock, a digital clock synthesizer is provided to which an output signal of the reference oscillator and a control signal are fed from the digital part in the form of a digital tuning word, the frequency of the reference oscillator being selected such that its order of magnitude is at least equal to the bandwidth of one or more of the reception bands used, and ~~none of its~~ harmonics do not occur in a reception channel.

Paragraph beginning on line 3 of page 3 has been amended as follows:

~~By virtue of the invention, it is easily possible to avoid~~ The invention prevents harmonics occurring in a reception channel, with the result that the shielding between the transmitter part and receiver part can be significantly reduced.

Paragraph beginning on line 8 of page 3 has been amended as follows:

In one ~~particular advantageous~~ embodiment, the clock synthesizer is embodied as a synthesizer with direct digital synthesis because as a result any frequency can be generated from any other frequency, and the frequency can also be finely adjusted.

Paragraph beginning on line 13 of page 3 has been amended as follows:

A further ~~advantageous~~ embodiment has a first frequency converter which is a fractional N divider with a sigma-delta modulator. This embodiment provides the advantage that it permits high-speed channel changes, fine-tuning ~~steps~~ and good phase changing values with high comparison frequencies even with a conventional structure.

Paragraph beginning on line 26 of page 3 has been amended as follows:

Another ~~expedient development~~ embodiment of the invention is defined in that an IF oscillator is provided to which a second phase locked loop with a phase discriminator and a second frequency converter is assigned, an output signal of the reference oscillator being supplied to the frequency discriminator, and a modulation signal and a fine-tuning signal being supplied to the frequency converter. As a result, a modulated signal can be advantageously conditioned. It may be advantageous here if a GMSK modulation signal of a finely adjustable sigma-delta synthesizer is supplied to the IF oscillator.

Paragraph beginning on line 1 of page 4 has been amended as follows:

The ~~concept according to the~~ invention permits the use of both the conventional heterodyne receiver and of a homodyne receiver in which the modulated RF reception signal and an output signal, in each case with the latter's frequency, of the channel synthesizer are fed to a reception mixer so that the intermediate frequency corresponds to the baseband.

Paragraph beginning on line 15 of page 4 has been deleted.

Paragraph beginning on line 21 of page 4 has been amended as follows:

According to Figure 1 ~~the drawing~~, a transceiver according to the invention includes ~~contains~~ a controller MPR and a baseband processing ~~means~~ device BBV, which are illustrated ~~here~~ in a single block designated as digital part DIT. A reference oscillator REO, which supplies an output signal S_{REF} is provided in a known fashion, and the ~~said~~ signal is then used in the way described below to acquire a control clock and to derive the channel frequencies necessary for the transceiver and transmitter. The output signal S_{REF} is then supplied to a digital synthesizer DDS, which expediently operates in accordance with digital direct synthesis. Such synthesizers are known, and a modern exemplary embodiment is described in the company literature CMOS, 125 MHz Complete DDS Synthesizer, AD 9850, Analog Devices, Inc. 1998, together with circuitry examples and functional explanations. ~~It is of particular importance for the present case that, in~~ In such a DDS synthesizer, any frequency can generate any desired other frequency, and fine adjustment is also possible using an AFC signal so that cheaper oscillators of any desired frequency, even ceramic oscillators or freewheeling oscillators, can be used as the reference oscillator. Reference oscillators have until now been one of the most expensive modules in radio telephones owing to the necessary precision and stability.

Paragraph beginning on line 9 of page 5 has been amended as follows:

The synthesizer DDS supplies a control clock f_{STE} to a micro controller of the digital part DIT, and receives from said block a control signal S_{AFC}, namely in the form of a digital tuning word, which both brings about the frequency conversion and the fine tuning to the precise clock frequency, which is carried out using a precise clock received from the base station, namely in the form of a digital tuning word. The output signal S_{REF} of the reference oscillator REO is also

fed to a phase lock loop which includes ~~contains~~ a first frequency converter FU1, a phase discriminator PD1, a low-pass filter, TP1 and a local channel oscillator EVO. The frequency converter FU1 is expediently embodied as a fractional N divider with sigma-delta modulator, and it receives a fine-tuning signal h_{AFC} and a channel signal S_{KAN} from the microprocessor block MPR, BBV. The output signal of the channel oscillator EVO is fed at the receiver end to a receiver mixer EMI. The radio-frequency signal S_{HAM} is supplied to this receiver mixer, ~~said~~ the radio-frequency signal S_{HAM} passing via an antenna ANT with a controllable change-over switch AUS, a bandpass filter BP2 and a low-noise amplifier LNA. Mixing is expediently carried out directly into the baseband, in accordance with modern concepts, i.e. the frequency of the mixing oscillator signal ~~always~~ corresponds precisely to the frequency of the radio-frequency signal S_{HAM}. The oscillator frequency at the mixer input can be the same as the direct frequency of the oscillator EVO, or equal to a frequency of the oscillator EVO which is converted, for example by means of a frequency converter. Receivers operating according to this principle are known as homodyn receivers. A detailed description of a signal-delta fractional N synthesizer can be found in "Delta-Sigma Modulation in Fractional-N Frequency Synthesis", EEE Journal of Solid-State Circuits, Vol. 28, No. 5, May 1993, pp 553-559.

Paragraph beginning on line 5 of page 6 has been amended as follows:

At the transmitter end, the output signal S_{EVO} of the channel oscillator EVO is fed to a transmitter mixer SME. The transmitter mixer is included ~~contained~~ in a phase locked loop which includes ~~contains~~ a controlled transmission oscillator SVO, a phase discriminator PD3 and a low-pass filter TP3, and a signal h_{MOD} is also supplied to the (third) phase discriminator PD3, in addition to the output signal S_{SMI}.

Paragraph beginning on line 13 of page 6 has been amended as follows:

The signal h_{MOD} constitutes the modulated output signal of an IF oscillator ZFO, which is likewise ~~contained~~ included in a (second) phase locked loop which also ~~contains~~ includes a second frequency converter FU2, a second phase discriminator PD2 and a second low-pass filter TP2. A modulation signal S_{MOD} and a fine-tuning signal g_{afc} are fed to the frequency converter FU2 by the microprocessor and baseband blocks MPR, BBV, and the output signal of the frequency converter FU2 passes to an input of the phase discriminator PD2 whose other input is supplied with the output signal S_{REF} of the reference oscillator REO.

In the Claims:

~~Patent claims~~

What is claimed is

1. (Amended) A transceiver, comprising:

~~having~~ an RF receiver~~, in particular UHF receiver,~~ with a digital signal processing device in a digital part ~~(DIT),~~ with an input part~~,~~;

at least one mixer; and

~~and~~ an intermediate frequency/baseband processing ~~means (BBV),~~ device having a local channel oscillator ~~(EVO)~~ to which a first phase locked loop with a phase discriminator ~~(PD1)~~ and an adjustable first frequency converter are assigned, and having a reference oscillator ~~(REO)~~ for the first phase locked loop and ~~the~~ a control clock ~~(f_{ST})~~ of the digital signal processing ~~means~~ device,

~~characterized in that,~~ wherein in order to acquire the control clock ~~(f_{STE})~~, a digital clock synthesizer ~~(DDS)~~ is provided to which an upward signal ~~(S_{REF})~~ of the reference oscillator ~~(REO)~~ is supplied, and a control signal ~~(S_{AFC})~~ is supplied by the digital part ~~(DIT)~~ in the form of a digital tuning word, the frequency ~~(f_{REO})~~ of the reference oscillator ~~(REO)~~ being selected such that its order of magnitude is at least equal to the bandwidth of one ~~of~~ or more of the reception bands used and ~~none of its~~ harmonics do not occur in a reception channel.

2. (Amended) The transceiver as claimed in claim 1, ~~characterized in that~~ wherein the clock synthesizer ~~(DDS)~~ is ~~embodied as~~ a synthesizer with direct digital synthesis.

3. (Amended) The transceiver as claimed in claim 1 ~~or 2~~, ~~characterized in that~~ wherein the first frequency converter ~~(FU1)~~ is a DDS synthesizer or a fractional N divider with a sigma-delta modulator.

4. (Amended) The transceiver as claimed in ~~one of claims 1 to 3, characterized in that~~ claim 1, wherein a fine-tuning signal ~~(h_{AFC})~~ is supplied to the first frequency converter ~~(FU1)~~ by the digital part ~~(DIT)~~.

5. (Amended) The transceiver as claimed in ~~one of claims 1 to 4, characterized in that~~ claim 1, further comprising an IF oscillator ~~(ZFO) is provided~~ to which a second phase locked loop with a phase discriminator ~~(PD2)~~ and a second frequency converter ~~(FU2)~~ is assigned, an output signal ~~(S_{REF})~~ of the reference oscillator ~~(REO)~~ being supplied to the phase discriminator, and a modulation signal ~~(S_{MOD})~~ and a fine-tuning signal ~~(g_{AFC})~~ being supplied to the frequency converter ~~(FU2)~~ by the digital part ~~(DIT)~~.

6. (Amended) The transceiver as claimed in ~~one of claims 1 to 5, characterized in that~~ claim 1, wherein the frequency converter ~~(FU2) which is~~ assigned to the IF oscillator ~~(ZFO)~~ is a DDS synthesizer or a fractional N divider with sigma-delta modulator.

7. (Amended) The transceiver as claimed in one ~~of claims 1 to 6, characterized in that~~ claim 1, wherein the modulation signal~~, for example for GMSK modulation,~~ is supplied to the ~~finely adjustable~~ IF oscillator frequency converter ~~(FU2)~~ from the digital part ~~(DIT)~~.

8. (Amended) The transceiver as claimed in ~~one of claims 1 to 7, characterized in that~~ claim 1, wherein the modulated IF signal is generated using frequency conversion, frequency division or DDS.

9. (Amended) The transceiver as claimed ~~in one of claims 1 to 8, characterized in that it is embodied as~~ claim 1, wherein the transciever is a homodyne receiver in which the modulated RF carrier ~~(S_{HAM})~~, and a direct or rearranged output signal~~, in each case with the frequency of said modulated RF carrier (S_{HAM})~~, of the local channel oscillator ~~(EVO)~~ are supplied to a reception mixer ~~(EMI)~~ so that the intermediate frequency corresponds to the baseband.

10. (Amended) The transceiver as claimed in ~~one of claims 5 to 9, characterized in that~~ claim 5, wherein the modulated output signal ~~(h_{MOD})~~ of the IF oscillator ~~(ZFO)~~ and the output signal of a transmission mixer ~~(SMI)~~ are fed to a phase discriminator ~~(PD3)~~, to which a signal of a controlled transmission oscillator ~~(SVO)~~ and an output signal ~~(S_{EVO})~~ of the local channel oscillator ~~(EVO)~~ are supplied.

Transceiver Having Digital Signal Processing

Abstract

A transceiver having an RF receiver, in particular VHF receiver, with digital signal processing in a digital part. The transceiver having an input part, at least one mixer and an intermediate frequency/baseband processing device, having a local channel oscillator, to which a first phase locked loop with a phase discriminator and an adjustable first frequency converter are assigned, and having a reference oscillator for the phase locked loop and the control clock of the digital signal processing device, in which, in order to acquire the control clock, a digital clock synthesizer is provided to which an output signal of the reference oscillator is supplied, and a control signal is supplied by the digital part in the form of a digital tuning word, the frequency of the reference oscillator being selected such that its order of magnitude is at least equal to the bandwidth of one or more of the reception bands used, and none of its harmonics occur in a reception channel.

Description

The invention relates to a transceiver having an RF receiver, in particular UHF receiver, with digital signal processing means in a digital part, with an input part, at least one mixer and an intermediate frequency/baseband processing means, and having a local channel oscillator to which a first phase locked loop with a phase discriminator and an adjustable first frequency converter are assigned, and having a reference oscillator for the phase locked loop and the control clock of the digital signal processing means.

In many radios, and in particular in radio telephones, the clock oscillator is a crystal oscillator with a relatively low frequency whose harmonics can occur in the reception band of the receiver.

GSM devices operate, for example, in the 900 MHz band, and in conventional embodiments the receiver has an intermediate frequency of 45 - 400 MHz and the transmitter operates with direct modulation of a carrier which is generated on the transmission frequency. A channel oscillator and a fixed frequency oscillator both use a 13 MHz crystal oscillator as a reference, the frequency of 13 MHz being used because the clock frequency which is required centrally by the GSM digital part relates to 13 MHz with 13/6 = 2.1666 MHz, and the channel raster frequency of 200 kHz, which is equal to the comparison frequency of the channel synthesizer, is also derived from it by simple frequency division. 13 MHz is thus the lowest possible reference oscillator frequency of each conventional GSM telephone.

The seventy-second harmonic of the 13 MHz oscillator occurs in the 936 MHz reception channel, and the seventy-third harmonic occurs in the 949 MHz reception channel. In particular in mobile phones which are highly miniaturized, the spatial proximity of the radio modules to the

receiver input and to the antenna results in a particular problem. Current specifications prescribe that interference frequencies at the 50 ohm receiver input must be less than 0.7 micro volts, for example. A customary 13 MHz crystal oscillator oscillates at an amplitude of approximately 1 volt, which means that harmonics of this oscillator may appear damped by more than 120 dB in the 900 MHz region at the receiver input. However, the high-speed silicon transistors which are customary today give rise to upper harmonic intervals of only approximately 60 dB in relation to the useful carrier in the 900 MHz region. Additional damping between the crystal oscillator and the receiver input of approximately 60 dB is thus necessary. Given the small spatial distances between these regions of at most 40 mm, this gives rise to an extreme level of expenditure on shielding in customary GSM mobile phones, i.e. to the use of sheet metal parts, metal housing etc. Attempts at solving this harmonic problem by means of switching measures alone, for example by means of harmonic filters, have only been partially successful because the harmonics are generally reflected by them and not destroyed, which in an extreme case can even lead to a situation in which critical harmonics are irradiated in an amplified form.

An object of the invention is therefore to provide a transceiver in which the aforesaid problem with harmonics of the reference oscillator is solved to the effect that costs, volume and weight of the device are reduced by eliminating or decreasing the expenditure on shielding.

This object is achieved with a transceiver of the type mentioned at the beginning in which, according to the invention, in order to acquire the control clock, a digital clock synthesizer is provided to which an output signal of the reference oscillator and a control signal are fed from the digital part in the form of a digital tuning word, the frequency of the

reference oscillator being selected such that its order of magnitude is at least equal to the bandwidth of one or more of the

reception bands used, and none of its harmonics occur in a reception channel.

By virtue of the invention, it is easily possible to avoid harmonics occurring in a reception channel, with the result that the shielding between the transmitter part and receiver part can be significantly reduced.

In one particular advantageous embodiment, the clock synthesizer is embodied as a synthesizer with direct digital synthesis because as a result any frequency can be generated from any other frequency, and the frequency can also be finely adjusted.

A further advantageous embodiment has a first frequency converter which is a fractional N divider with sigma-delta modulator. This embodiment provides the advantage that it permits high-speed channel changes, fine-tuning steps and good phase changing values with high comparison frequencies even with a conventional structure.

A fine-tuning signal is advantageously supplied to the first frequency converter by the digital part, as a result of which a cheaper reference oscillator can be used which does not require any fine tuning. In principle, a fine-tuning signal can advantageously be supplied to all the frequency converters used.

Another expedient development of the invention is defined in that an IF oscillator is provided to which a second phase locked loop with a phase discriminator and a second frequency converter is assigned, an output signal of the reference oscillator being supplied to the frequency discriminator, and a modulation signal and a fine-tuning signal being supplied to the frequency converter. As a result, a modulated signal can be advantageously conditioned. It may be advantageous here if a GMSK modulation signal of a finely adjustable sigma-delta synthesizer is supplied to the IF oscillator

The concept according to the invention permits the use of both the conventional heterodyne receiver and of a homodyne receiver in which the modulated RF reception signal and an output signal, in each case with the latter's frequency, of the channel synthesizer are fed to a reception mixer so that the intermediate frequency corresponds to the baseband.

A simple and cost-effective connection between the transmitter and receiver is obtained if the modulated output signal of the IF oscillator and the output signal of a transmission mixer are fed to a phase discriminator to which a signal of a controlled transmission oscillator and an output signal of the local channel oscillator are fed.

The invention, together with further advantages, is explained in more detail below with reference to an exemplary embodiment which is illustrated in the drawing. In the said drawing, the single figure shows a basic, simplified block diagram of a transceiver according to the invention.

According to the drawing, a transceiver according to the invention contains a controller MPR and a baseband processing means BBV, which are illustrated here in a single block designated as digital part DIT. A reference oscillator REO, which supplies an output signal S_{REF} is provided in a known fashion, and said signal is then used in the way described below to acquire a control clock and to derive the channel frequencies necessary for the transceiver and transmitter. The output signal S_{REF} is then supplied to a digital synthesizer DDS, which expediently operates in accordance with digital direct synthesis. Such synthesizers are known, and a modern exemplary embodiment is described in the company literature CMOS, 125 MHz Complete DDS Synthesizer, AD 9850, Analog Devices, Inc. 1998, together with circuitry examples and functional explanations. It is of particular importance for the present case that, in

such a DDS

synthesizer, any frequency can generate any desired other frequency, and fine adjustment is also possible using an AFC signal so that cheaper oscillators of any desired frequency, even ceramic oscillators or freewheeling oscillators, can be used as the reference oscillator. Reference oscillators have until now been one of the most expensive modules in radio telephones owing to the necessary precision and stability.

The synthesizer DDS supplies a control clock f_{STE} to a micro controller of the digital part DIT, and receives from said block a control signal S_{AFC}, namely in the form of a digital tuning word, which both brings about the frequency conversion and the fine tuning to the precise clock frequency, which is carried out using a precise clock received from the base station, namely in the form of a digital tuning word. The output signal S_{REF} of the reference oscillator REO is also fed to a phase lock loop which contains a first frequency converter FU1, a phase discriminator PD1, a low-pass filter, TP1 and a local channel oscillator EVO. The frequency converter FU1 is expediently embodied as a fractional N divider with sigma-delta modulator, and it receives a fine-tuning signal h_{AFC} and a channel signal S_{KAN} from the microprocessor block MPR, BBV. The output signal of the channel oscillator EVO is fed at the receiver end to a receiver mixer EMI. The radio-frequency signal S_{HAM} is supplied to this receiver mixer, said radio-frequency signal S_{HAM} passing via an antenna ANT with a controllable change-over switch AUS, a bandpass filter BP2 and a low-noise amplifier LNA. Mixing is expediently carried out directly into the baseband, in accordance with modern concepts, i.e. the frequency of the mixing oscillator signal always corresponds precisely to the frequency of the radio-frequency signal S_{HAM}. The oscillator frequency at the mixer input can be the same as the direct frequency of the oscillator EVO, or equal to a frequency of the

oscillator EVO which is converted, for example by means of a frequency converter. Receivers operating according to this principle are known as homodyn receivers. A detailed description of a signal-delta

fractional N synthesizer can be found in "Delta-Sigma Modulation in Fractional-N Frequency Synthesis", EEE Journal of Solid-State Circuits, Vol. 28, No. 5, May 1993, pp 553-559.

At the transmitter end, the output signal S_{EVO} of the channel oscillator EVO is fed to a transmitter mixer SME. The transmitter mixer is contained in a phase locked loop which contains a controlled transmission oscillator SVO, a phase discriminator PD3 and a low-pass filter TP3, and a signal h_{MOD} is also supplied to the (third) phase discriminator PD3, in addition to the output signal S_{SMI}.

The signal h_{MOD} constitutes the modulated output signal of an IF oscillator ZFO, which is likewise contained in a (second) phase locked loop which also contains a second frequency converter FU2, a second phase discriminator PD2 and a second low-pass filter TP2. A modulation signal S_{MOD} and a fine-tuning signal g_{afc} are fed to the frequency converter FU2 by the microprocessor and baseband blocks MPR, BBV, and the output signal of the frequency converter FU2 passes to an input of the phase discriminator PD2 whose other input is supplied with the output signal S_{REF} of the reference oscillator REO.

When still at the transmitter end, an output signal of the controlled transmission oscillator SVO is finally supplied to a transmission amplifier SEV, and from here to the antenna change-over switch AUS or the antenna ANT via a low-pass filter TP4.

The invention is particularly suitable for transceivers in which the problems mentioned at the beginning in terms of the harmonics are significant. Practical embodiments have proven expedient for radio telephones which operate in the 900, 1800, 1900 and 2000 MHz ranges, and thus in the GSM 900, GSM 1800, GSM 1900 and IMT-2000 systems (UMTS). In what is referred to as multimode devices, it may be necessary to select a

reference oscillator frequency whose harmonics occur in none of the reception bands used.

Patent claims

1. A transceiver having an RF receiver, in particular UHF receiver, with digital signal processing in a digital part (DIT), with an input part, at least one mixer and an intermediate frequency/baseband processing means (BBV), having a local channel oscillator (EVO) to which a first phase locked loop with a phase discriminator (PD1) and an adjustable first frequency converter are assigned, and having a reference oscillator (REO) for the phase locked loop and the control clock (f_{ST}) of the digital signal processing means, characterized in that, in order to acquire the control clock (f_{STE}), a digital clock synthesizer (DDS) is provided to which an upward signal (S_{REF}) of the reference oscillator (REO) is supplied, and a control signal (S_{AFC}) is supplied by the digital part (DIT) in the form of a digital tuning word, the frequency (f_{REO}) of the reference oscillator (REO) being selected such that its order of magnitude is at least equal to the bandwidth of one of more of the reception bands used and none of its harmonics occur in a reception channel.

2. The transceiver as claimed in claim 1, characterized in that the clock synthesizer (DDS) is embodied as a synthesizer with direct digital synthesis.

3. The transceiver as claimed in claim 1 or 2, characterized in that the first frequency converter (FU1) is a DDS synthesizer or a fractional N divider with sigma-delta modulator.

4. The transceiver as claimed in one of claims 1 to 3, characterized in that a fine-tuning signal (h_{AFC}) is

supplied to the first frequency converter (FU1) by the digital part (DIT).

5. The transceiver as claimed in one of claims 1 to 4, characterized in that an IF oscillator (ZFO) is provided to which a second phase locked loop with a phase discriminator (PD2) and a second frequency converter (FU2) is assigned, an output signal (S_{REF}) of the reference oscillator (REO) being supplied to the phase discriminator, and a modulation signal (S_{MOD}) and a fine-tuning signal (g_{AFC}) being supplied to the frequency converter (FU2) by the digital part (DIT).

6. The transceiver as claimed in one of claims 1 to 5, characterized in that the frequency converter (FU2) which is assigned to the IF oscillator (ZFO) is a DDS synthesizer or a fractional N divider with sigma-delta modulator.

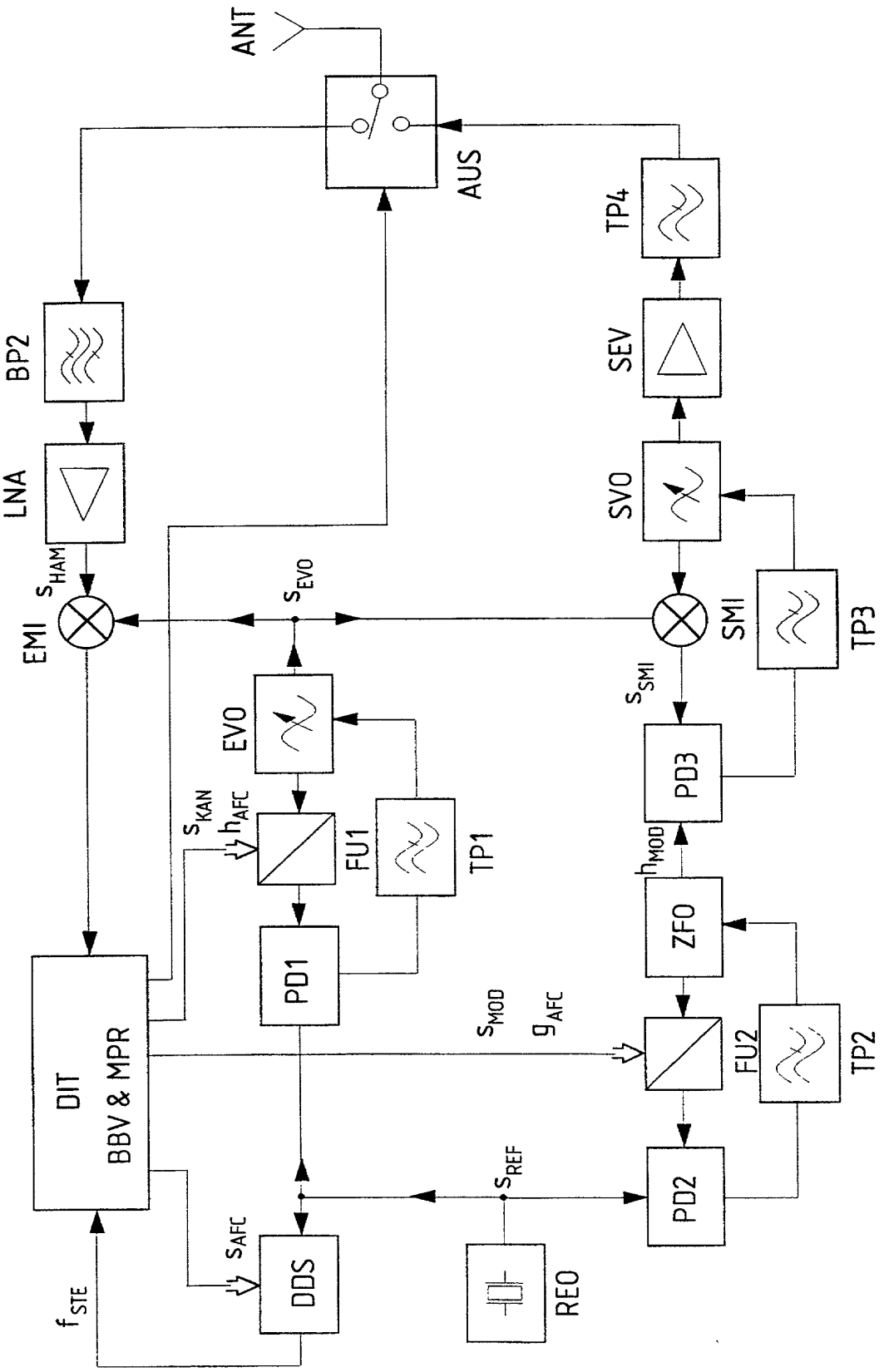
7. The transceiver as claimed in one of claims 1 to 6, characterized in that the modulation signal, for example for GMSK modulation, is supplied to the finely adjustable IF oscillator frequency converter (FU2) from the digital part (DIT).

8. The transceiver as claimed in one of claims 1 to 7, characterized in that the modulated IF signal is generated using frequency conversion, frequency division or DDS.

9. The transceiver as claimed in one of claims 1 to 8, characterized in that it is embodied as a homodyne receiver in which the modulated RF carrier (S_{HAM}), and a direct or rearranged output signal, in each case with the frequency of said modulated RF carrier (S_{HAM}), of the local channel oscillator (EVO) are supplied to a reception mixer (EMI) so that the intermediate frequency corresponds to baseband.

10. The transceiver as claimed in one of claims 5 to 9,characterized in that the modulated output signal (h_{MOD}) of the IF oscillator (ZFO) and the output

signal of a transmission mixer (SMI) are fed to a phase discriminator (PD3), to which a signal of a controlled transmission oscillator (SVO) and an output signal (S_{EVO}) of the local channel oscillator (EVO) are supplied.


ANT
AUS
BP2
LNA
EMI
s_{HAM}
s_{EVO}
EVO
s_{KAN}
h_{AFC}
FU1
TP1
PD1
DIT
BBV & MPR
s_{MOD}
g_{AFC}
s_{AFC}
DDS
f_{STE}
s_{REF}
REO
TP4
SEV
SVO
SMI
TP3
s_{SMI}
PD3
h_{MOD}
ZFO
FU2
TP2
PD2

Declaration and Power of Attorney For Patent Application
Erklärung Für Patentanmeldungen Mit Vollmacht
German Language Declaration

Als nachstehend benannter Erfinder erkläre ich hiermit an Eides Statt:

dass mein Wohnsitz, meine Postanschrift, und meine Staatsangehörigkeit den im Nachstehenden nach meinem Namen aufgeführten Angaben entsprechen,

dass ich, nach bestem Wissen der ursprüngliche, erste und alleinige Erfinder (falls nachstehend nur ein Name angegeben ist) oder ein ursprünglicher, erster und Miterfinder (falls nachstehend mehrere Namen aufgeführt sind) des Gegenstandes bin, für den dieser Antrag gestellt wird und für den ein Patent beantragt wird für die Erfindung mit dem Titel:

Sendeempfaenger

deren Beschreibung

(zutreffendes ankreuzen)
☐ hier beigefügt ist.
☒ am 01.03.2000 als
PCT internationale Anmeldung
PCT Anmeldungsnummer PCT/DE00/00614
eingereicht wurde und am _____
abgeändert wurde (falls tatsächlich abgeändert).

Ich bestätige hiermit, dass ich den Inhalt der obigen Patentanmeldung einschliesslich der Ansprüche durchgesehen und verstanden habe, die eventuell durch einen Zusatzantrag wie oben erwähnt abgeändert wurde.

Ich erkenne meine Pflicht zur Offenbarung irgendwelcher Informationen, die für die Prüfung der vorliegenden Anmeldung in Einklang mit Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) von Wichtigkeit sind, an.

Ich beanspruche hiermit ausländische Prioritätsvorteile gemäss Abschnitt 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 119 aller unten angegebenen Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde, und habe auch alle Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde nachstehend gekennzeichnet, die ein Anmeldedatum haben, das vor dem Anmeldedatum der Anmeldung liegt, für die Priorität beansprucht wird.

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Sendeempfaenger

the specification of which

(check one)
☐ is attached hereto.
☒ was filed on 01.03.2000 as
PCT international application
PCT Application No. PCT/DE00/00614
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Form PTO-FB-240 (8-83) Patent and Trademark Office-U.S. DEPARTMENT OF COMMERCE

German Language Declaration

Prior foreign appplications
Priorität beansprucht

			Priority Claimed	
19911147.2	DE	12.03.1999	☐	☐
(Number)	(Country)	(Day Month Year Filed)	Yes	No
(Nummer)	(Land)	(Tag Monat Jahr eingereicht)	Ja	Nein
			☐	☐
(Number)	(Country)	(Day Month Year Filed)	Yes	No
(Nummer)	(Land)	(Tag Monat Jahr eingereicht)	Ja	Nein
			☐	☐
(Number)	(Country)	(Day Month Year Filed)	Yes	No
(Nummer)	(Land)	(Tag Monat Jahr eingereicht)	Ja	Nein

Ich beanspruche hiermit gemäss Absatz 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 120, den Vorzug aller unten aufgeführten Anmeldungen und falls der Gegenstand aus jedem Anspruch dieser Anmeldung nicht in einer früheren amerikanischen Patentanmeldung laut dem ersten Paragraphen des Absatzes 35 der Zivilprozeßordnung der Vereinigten Staaten, Paragraph 122 offenbart ist, erkenne ich gemäss Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) meine Pflicht zur Offenbarung von Informationen an, die zwischen dem Anmeldedatum der früheren Anmeldung und dem nationalen oder PCT internationalen Anmeldedatum dieser Anmeldung bekannt geworden sind.

I hereby claim the benefit under Title 35. United States Code. §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §122, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occured between the filing date of the prior application and the national or PCT international filing date of this application.

PCT/DE00/00614	01.03.2000		
(Application Serial No.) (Anmeldeseriennummer)	(Filing Date D, M, Y) (Anmeldedatum T, M, J)	(Status) (patentiert, anhängig, aufgegeben)	(Status) (patented, pending, abandoned)
(Application Serial No.) (Anmeldeseriennummer)	(Filing Date D,M,Y) (Anmeldedatum T, M; J)	(Status) (patentiert, anhängig, aufgeben)	(Status) (patented, pending, abandoned)

Ich erkläre hiermit, dass alle von mir in der vorliegenden Erklärung gemachten Angaben nach meinem besten Wissen und Gewissen der vollen Wahrheit entsprechen, und dass ich diese eidesstattliche Erklärung in Kenntnis dessen abgebe, dass wissentlich und vorsätzlich falsche Angaben gemäss Paragraph 1001, Absatz 18 der Zivilprozessordnung der Vereinigten Staaten von Amerika mit Geldstrafe belegt und/oder Gefängnis bestraft werden koennen, und dass derartig wissentlich und vorsätzlich falsche Angaben die Gültigkeit der vorliegenden Patentanmeldung oder eines darauf erteilten Patentes gefährden können.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

German Language Declaration

VERTRETUNGSVOLLMACHT: Als benannter Erfinder beauftrage ich hiermit den nachstehend benannten Patentanwalt (oder die nachstehend benannten Patentanwälte) und/oder Patent-Agenten mit der Verfolgung der vorliegenden Patentanmeldung sowie mit der Abwicklung aller damit verbundenen Geschäfte vor dem Patent- und Warenzeichenamt: *(Name und Registrationsnummer anführen)*

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*

Customer No.

And I hereby appoint

Telefongespräche bitte richten an:
(Name und Telefonnummer)

Direct Telephone Calls to: *(name and telephone number)*

Ext. _____

Postanschrift

Send Correspondence to:

Morrison and Foerster LLP
2000 Pennsylvania Ave., NW 20006-1888 Washington, DC
Telephone: (001) 202 887 1500 and Facsimile (001) 202 887 0763
or
Customer No.

Voller Name des einzigen oder ursprünglichen Erfinders: THOMAS MOLIERE	Full name of sole or first inventor: THOMAS MOLIERE
Unterschrift des Erfinders Datum Thomas Moliere 10th Dec 2001	Inventor's signature Date Thomas Moliere 10th Dec 2001
Wohnsitz MUENCHEN,	Residence MUENCHEN,
Staatsangehörigkeit DE DE X	Citizenship DE
Postanschrift JOHANN-FICHTE-STR.11/13 80805 MUENCHEN	Post Office Addess JOHANN-FICHTE-STR.11/13 80805 MUENCHEN
Voller Name des zweiten Miterfinders (falls zutreffend):	Full name of second joint inventor, if any:
Unterschrift des Erfinders Datum	Second Inventor's signature Date
Wohnsitz ,	Residence ,
Staatsangehörigkeit	Citizenship
Postanschrift	Post Office Address

(Bitte entsprechende Informationen und Unterschriften im Falle von dritten und weiteren Miterfindern angeben).

(Supply similar information and signature for third and subsequent joint inventors).